Lab 5: Lab Report

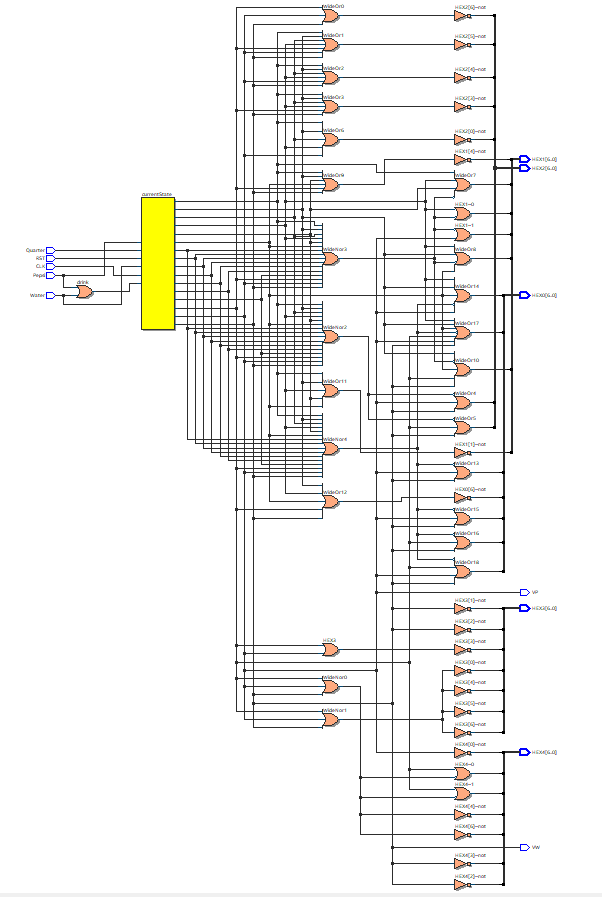
John Bretz

Dr. Varnell

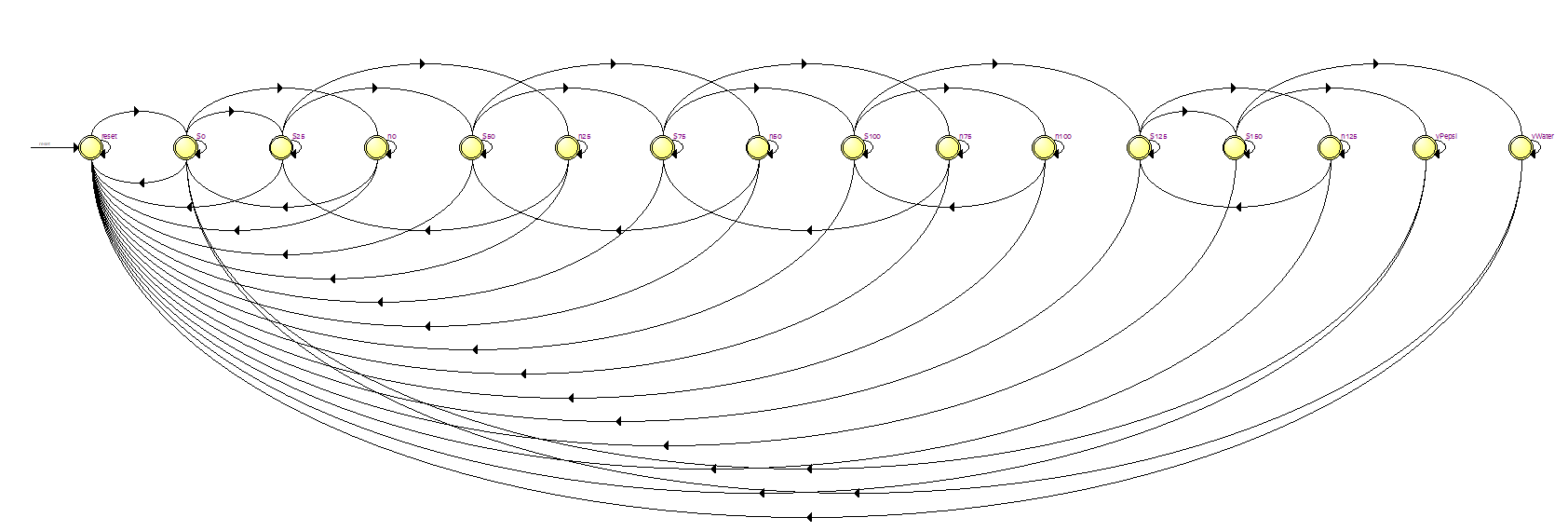
Abstract

This project has four main components. All the data is stored in the register process and on a rising clock edge the system will try to advance to the next state if the inputs will allow it. In the next state logic process, whenever only a quarter is on, the change in the system will increase until saturating at $1.50. If water or Pepsi it toggled and there is enough change then the system will vend the respective drink and go back to the state with no change. If there is not enough change the machine will show the cost and go back to the previous state. The system will ignore inputs if more than one switch is toggled at a time. The output logic will print the appropriate text to the seven-segment based off the machine’s current state. Finally a slow clock, process is used to slow down the internal clock to have a period of one second in

Circuits

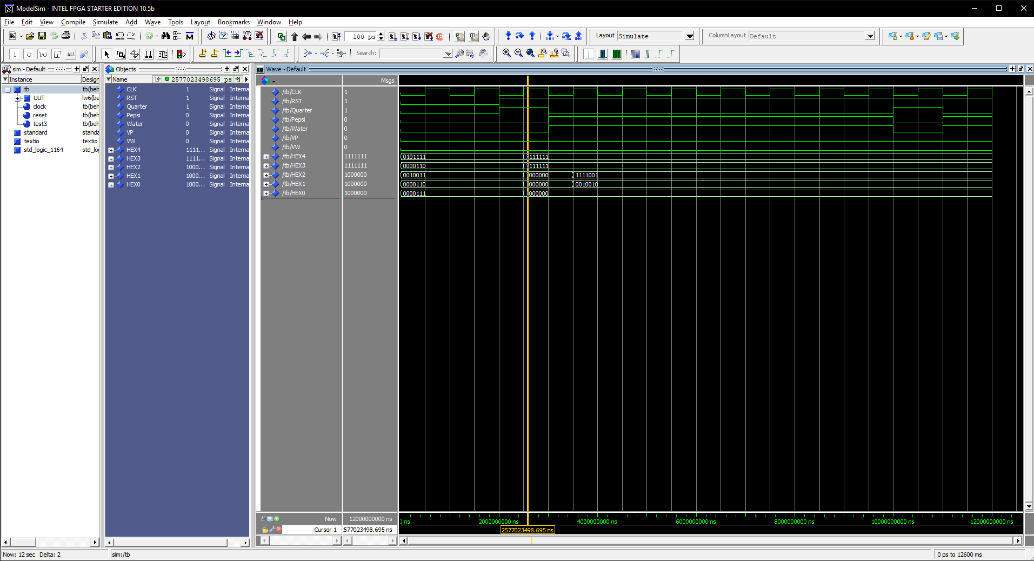
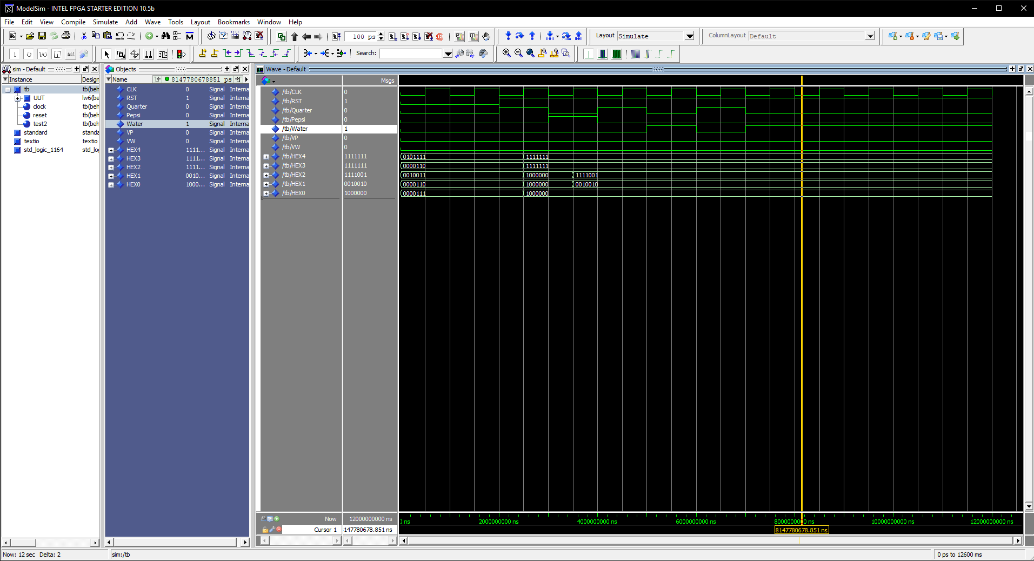
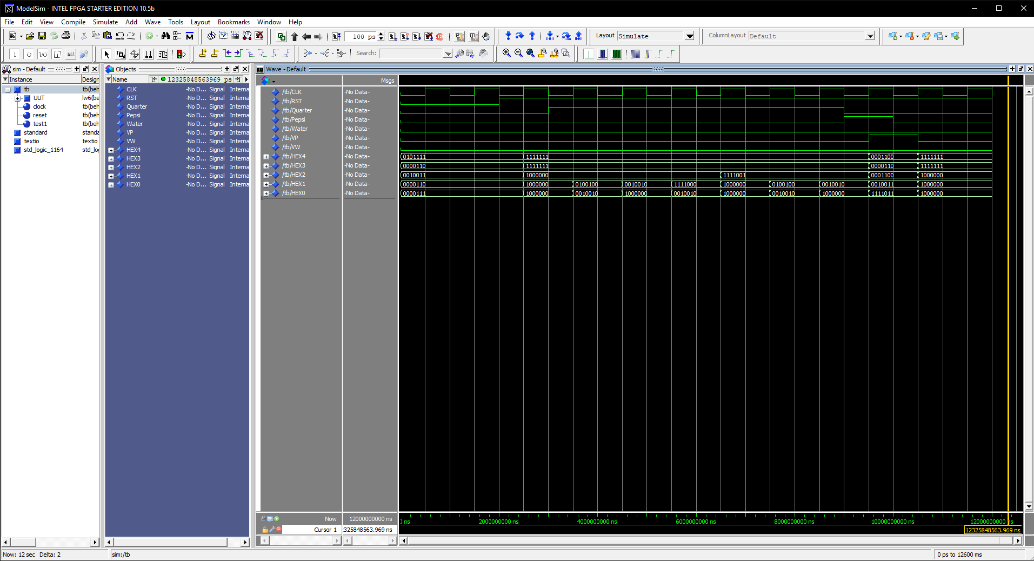


RTL schematic

 The State machine

Simulations

All inputs and timeframes were chosen based off the unit tests given in the lab manual.



Typical use case simulation

Random user input simulation

Random user input with simultaneous button presses

Conclusion

This lab reinforced my understanding of state machines and using types within Quartus. I also learned about the wonder that is using attributes to assign pins.